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ABSTRACT

A high-performance, high I/O ball grid array substrate, designed for integrated circuit flip-chip assembly and having two patterned metal layers, comprising: an insulating layer having a first surface, a second surface and a plurality of vias filled with metal. Said first surface having one of said metal layers attached to provide electrical ground potential, and having a plurality of electrically insulated openings for outside electrical contacts. An outermost insulating film protecting the exposed surface of said ground layer, said film having a plurality of openings filled with metal suitable for solder ball attachment. Said second surface having the other of said metal layers attached, portions thereof being configured as a plurality of electrical signal lines, further portions as a plurality of first electrical power lines, and further portions as a plurality of second electrical power lines, selected signal and power lines being in contact with said vias. Said signal lines being distributed relative to said first power lines such that the inductive coupling between them reaches at least a minimum value, providing high mutual inductances and minimized effective self-inductance. Said signal lines further being electromagnetically coupled to said ground metal such that cross talk between signal lines is minimized. And an outermost insulating film protecting the exposed surfaces of said signal and power lines, said film having a plurality of openings filled with metal suitable for contacting selected signal and power lines and chip solder bumps.